Influence of the polymer dielectric characteristics on the performance of a quaterthiophene organic field-effect transistor

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Organic field-effect transistors were fabricated with quaterthiophene as the active material and various polymeric dielectrics as the gate insulator. The conduction parameters such as mobility, threshold voltage, subthreshold swing, the maximum density of surface states etc. were found out. The performances of the devices were compared with respect to the dielectric constant, thickness and surface morphology of the gate insulator and the leakage current through the gate. Out of the three dielectrics investigated *viz.* parylene-C, cyanoethylpullulan and poly(methylmethacrylate); parylene-C was found to be best suited for applications in organic FETs.

1. Introduction

Research on organic field effect transistors (OFET) has been rapidly growing in recent years. They are potential candidates for use in a wide range of applications in low cost and large area electronics [1]. Low process temperature of these devices may pave way for organic FETs to be integrated on inexpensive plastic substrates. The prospect of flexible, unbreakable, extremely low weight flat panel displays at low cost has spurred significant commercial interest. However, despite the considerable progress made in recent years, achieving high carrier mobilities with organic semiconductors remains inherently difficult. The formation of electronic bands is very limited and therefore the highest mobilities are in the range 1–3 $cm^2\ V^{-1}\ s^{-1}$ [1–3]. Efforts to increase the mobility limits have been focussed on the development of better semiconductor materials and understanding their morphology and mechanism of charge transport. Nevertheless it has been noticed that the interaction between the insulator and the semiconducting materials plays an important role in the carrier transport because the morphology of the thin interfacial region is likely to be different from the bulk and the interface has been found to affect the ordering [4–7]. Though certain organic dielectrics have been employed as gate materials, most of the studies on organic FETs are still made with SiO_2 as the gate dielectric. However to realize low cost and large area electronics, using organic semiconductors, it is highly desirable that SiO_2 may be substituted with an organic dielectric. In this paper, we evaluate the performance of three organic dielectrics, namely cyanoethylpullulan (CyEP), poly(methylmethacrylate) (PMMA), and parylene-C in an organic FET with quaterthiophene (4T) as a model active material.

α-oligothiophenes (nT, where n denotes the number of thiophene units) and in particular quaterthiophene (4T) and sexithiophene (6T) have recently received considerable attention as promising organic semiconducting materials [8]. The electrical, optical and structural properties of 4T has been extensively studied for a better comprehension of optical and electrical properties of conducting polythiophenes [9–11].

2. Experimental

Indium Tin Oxide (ITO) coated glass slides (Merck, $R_s < 15\ \Omega/\gamma$) were used as the substrates. The ITO was selectively etched to form the electrical contacts for the gate dielectric and contacts for the source and drain electrodes. The patterned substrates were carefully cleaned using several rounds of ultrasonic rinsing in dilute detergent, deionized water, ethyl alcohol, and acetone. After drying in a flow of nitrogen, the substrates were baked in an oven for one hour at 100°C. UV-ozone cleaning for 10 min was performed just before the fabrication of the devices. PMMA was deposited from a solution of toluene

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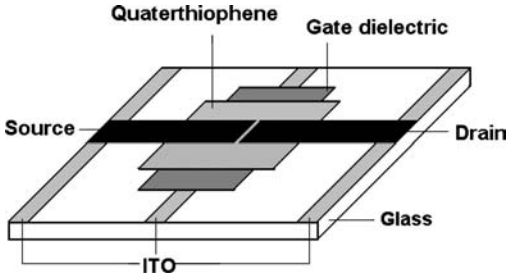

Figure 1 Schematic diagram of the quaterthiophene FET used in this study.

and the film was annealed at 180°C for two hours. The concentration was 100 mg/ml. CyEP was deposited by spin coating from a solution of acetonitrile and N, N, dimethylformamide (DMF) (1:1). The concentration was 60 mg/ml. The films were annealed at 100°C for one hour in an oven. Parylene-C was deposited by vacuum evaporation of di-para-xylylene in a Para Tech parylene coating equipment. In this process, the dimer is converted into a gaseous monomer that condenses and polymerizes on substrates at room temperature. Quaterthiophene (obtained from Aldrich) was evaporated onto the polymer films using a thermal evaporation plant attached to a MBRAUN 200B glove box. The deposition was performed under a pressure of ca. 10^{-6} mb and at a rate of 0.1–0.2 nm per second, monitored by an Edwards FTM 7 quartz oscillator. The thickness of the 4T films was 100 nm. To complete the FET structure, gold source and drain electrodes were deposited over the 4T layer using a shadow mask under a pressure of 10^{-6} mb and at a rate of 0.01–0.02 nm per second. The gold electrodes had a thickness of 50 nm. The channel length was 120 μm and the channel width was 5 mm. During all the evaporations, the substrates were held at room temperature. A schematic representation of our device is given in Fig. 1.

The electrical characterization of the devices was done in Ar atmosphere inside the glove box, without the devices being exposed to the air. A combination of a Keithley 2400 SMU and a Keithley 236 SMU was used to study the FET characteristics. Atomic Force microscope (AFM) images of insulator film surfaces (over ITO) were recorded in contact mode on a PICOAFM scanner (Molecular imaging Inc.). The capacitance values of the dielectric films were determined by a Solartron 1250 frequency response analyzer and a Solartron 1286 electrochemical interface, by employing a sandwich structure of the film with evaporated Al electrodes. The thickness of the 4T film and the dielectric films were measured by a Talystep 223-7 stylus profilometer.

3. Results and discussion

The transistor characteristics of the quaterthiophene FETs fabricated with the three dielectrics PMMA, CyEP and parylene-C are shown in Fig. 2. The saturated drain current $I_{d,\mathrm{sat}}$ is given by [12]

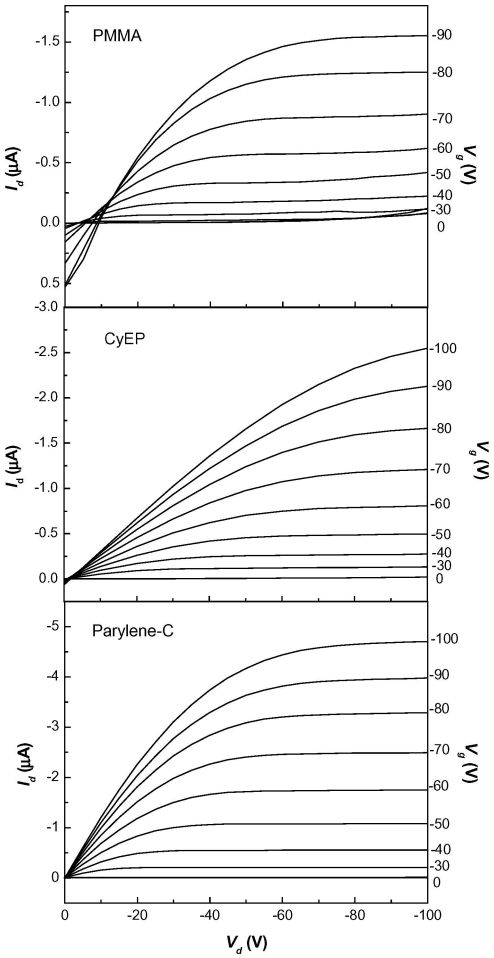

Figure 2 Transistor characteristics of the quaterthiophene FETs fabricated using the different dielectrics: PMMA, CyEP, Parylene-C.

$$I_{d,\mathrm{sat}} = \frac{W}{2L} C_i \mu_{\mathrm{FE}} (V_g - V_t)^2 \tag{1}$$

where W is the width of the channel, L is the length of the channel, C_i is the capacitance of the insulator layer per unit area, μ_{FE} is the field effect mobility, V_g is the gate voltage and V_t, the threshold voltage. V_t accounts for various voltage shifts across the insulator–semiconductor interface, namely work function difference between the gate and the semiconductor, fixed charges in the insulator, and the bulk conductivity of the semiconductor [13]. The field effect mobility μ_{FE} can be estimated from the slope of a plot between $|I_{d,\mathrm{sat}}|^{0.5}$ *vs.* V_g. The extrapolated x-intercept of this plot yields the value of the threshold voltage. The respective plots are given in Fig. 3.

The small positive current at $V_d = 0$, which increases with V_g is due to the leakage between source-drain and gate electrodes through the insulating layer [14]. This current comes from leakages outside the channel of the transistor. The leakage current starts from the gate, passes through the insulator and comes back to the grounded source via the drain. It forms a current that flows even at

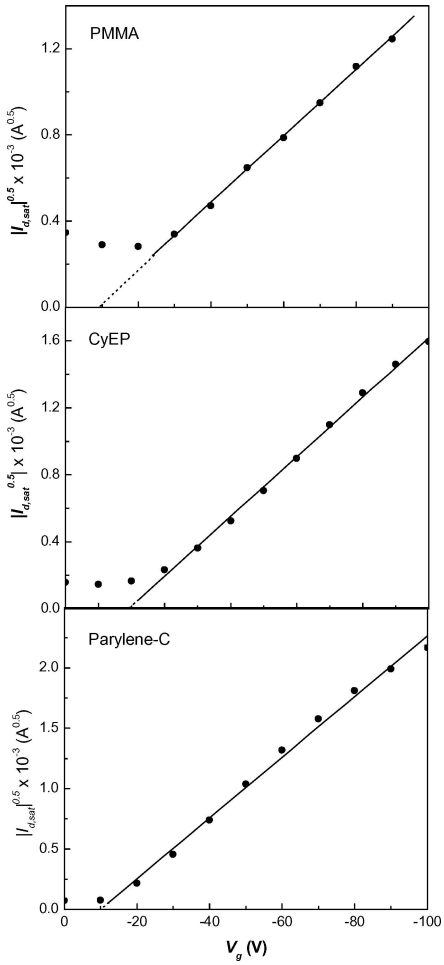

Figure 3 Plots of $|I_{d,\mathrm{sat}}|^{0.5}$ *vs.* V_g for the quaterthiophene FETs fabricated using the different dielectrics PMMA, CyEP, Parylene-C.

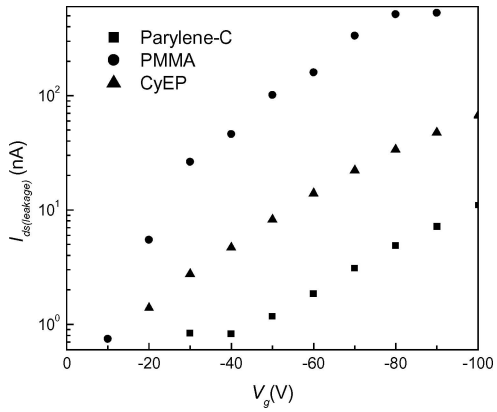

Figure 4 Plot of variation of $I_{ds,\mathrm{leakage}}$ *vs.* V_g for the quaterthiophene FETs fabricated using the different dielectrics PMMA, CyEP, Parylene-C.

zero drain voltage, in the direction from drain to source. That is why the sign of this current is opposite to that of the "normal" drain current. This is detrimental to the transistor performance. By using proper patterning of the gate electrode, or of the semiconductor channel, we can control this leakage. However this gives a measure of the quality of an organic dielectric to be used as a gate dielectric in a FET. Fig. 4 gives the variation of this leakage current with V_g for all the three devices.

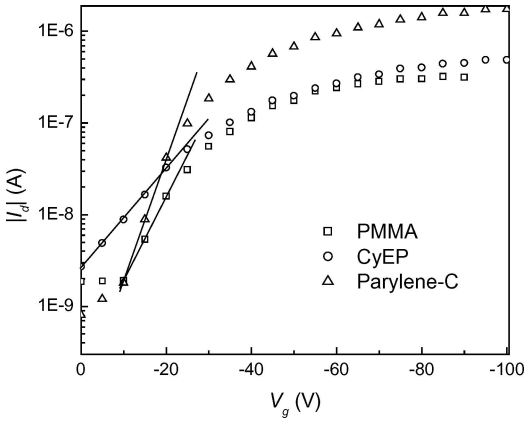

Figure 5 Transfer characteristics of the quaterthiophene FETs fabricated using the different dielectrics PMMA, CyEP, Parylene-C.

The channel conductivity σ can be estimated from the plot of I_d *vs.* V_d at zero gate voltage. Alternatively,

$$\sigma = N_p q \mu_{\mathrm{FE}} \tag{2}$$

where N_p is the concentration of charge carriers and q is the electronic charge. Equation 2 can be used to deduce the carrier concentration. Fig. 5 shows the transfer characteristic of the device from which we can calculate the inverse subthreshold slope S, given by

$$S = \left[\frac{d\log(I_d)}{dV_g}\right]^{-1} \tag{3}$$

Further analysis is possible from the subthreshold slope calculation. The maximum number of interface traps present can be calculated using Equation 4; assuming that the densities of deep bulk states and interface states are independent of energy [15].

$$N_{ss}^{\max} = \left[\frac{S.\log(e)}{\mathrm{kT}/q} - 1\right]\frac{C_i}{q} \tag{4}$$

where $N_{ss}^{\max}$ is the maximum number of interface states, k is the boltzman constant and T is the absolute temperature.

Fig. 6 shows the AFM images of the three insulator surfaces. The rms value of the surface roughness is found out in each case. In fact the surface roughness of the base ITO film critically influences the performance of the device fabricated upon it [16]. However this is not expected to play an important role in our devices since the dielectric films are all reasonably thick. Table I gives the values of dielectric constant (ε), thickness (d), C_i, and surface roughness (r) for the three insulator films. Table II gives the values of μ_{FE}, V_t, σ, N_p, S and $N_{ss}^{\max}$ for the quaterthiophene FETs fabricated using these three insulator films.

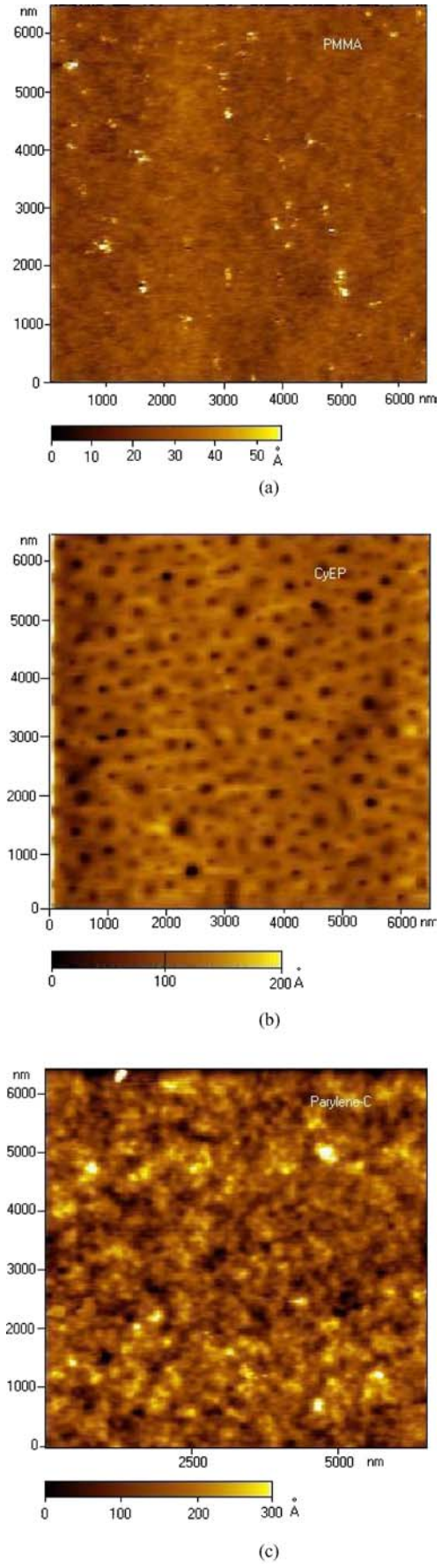

Figure 6 AFM images of the surface of the different dielectric films on ITO.

TABLE I Tabulation of the dielectric constant (ε), thickness (d), capacitance per unit area (C_i) and RMS value of surface roughness (r) of each insulator film used in this study

Dielectric	Dielectric Constant (ε)	Thickness (μm)	C_i (nFcm^{-2})	RMS surface roughness (Å)
PMMA	3.6	0.9	4	4
CyEP	18.5	0.9	20	28
Parylene-C	3.2	0.6	5	48

The PMMA device has the highest leakage current, amounting to hundreds of nanoamperes. This leakage is detrimental to the transistor performance because it prevents the device from reaching the high drain currents. The dielectric constant of PMMA is 3.6, which is also not favorable for high mobility. However the PMMA forms a very smooth film with roughness of only 4 Å. This helps the ordered growth of the semiconductor as can be seen from the comparatively better conductivity, and as a result, a good mobility value of 2.9×10^{-3} cm^2 V^{-1} s^{-1} is obtained. The inverse subthreshold swing is 11 V/dec and the maximum density of surface states derived from Equation 4 is 4.7×10^{12} eV^{-1} cm^{-2}.

The behavior of the CyEP device is rather complicated. Its low mobility value (0.8×10^{-3} cm^{2}V^{-1} s^{-1}) compared to the other two devices is a direct result of many competing mechanisms. CyEP has a high dielectric constant, 18.5 [14]. However the device has an appreciable leakage through the gate. A disadvantage of the high dielectric constant materials is the energetic disorder due to the localized states because of high dipolar disorder. The insulator is not only capable of affecting the morphology of the semiconductor layer, but can also change the density of states by local polarization effects. Carrier localization is enhanced by insulators with large permittivities, due to the random dipole field present at the interface [17]. The high dielectric constant of CyEP results from the presence of pendent groups with high dipolar moment. The surface roughness clearly helps increase the disorder, and affects the uniform growth of the semiconductor. As a result of all these mechanisms, the CyEP device exhibits a low mobility. The high subthreshold swing of 18 V/dec leads to a high interfacial trap density of 3.9×10^{13} eV^{-1} cm^{-2}. We note that high mobility values have been reported for α-sexithienylene FET with CyEP as gate dielectric [14, 18]. But in those cases the thickness of the gate insulator was very high, ranging to several micrometers. However such very thick films are not useful for the envisioned applications for organic thin film transistors in large area electronics.

The parylene-C device has the highest mobility of 6.1×10^{-3} cm^2 V^{-1} s^{-1}. The deposition process of parylene yields a robust and pinhole free film. Therefore it has the lowest leakage current and consequently the highest drain currents. Its highly rough surface hinders the ordered growth of the semiconductor, leading to low conductivity. Also in the present study, parylene had a lower thickness than the other two dielectric layers.

TABLE II Tabulation of field-effect mobility (μ_{FE}), threshold voltage (V_t), conductivity (σ), hole concentration (N_p), subthreshold swing(S) and maximum density of interfacial states(N_{ss}^{max}) for the quaterthiophene FETs fabricated using the different dielectrics

Dielectric	$\mu_{FE} \times 10^{-3}$ $cm^2V^{-1}s^{-1}$	V_t (V)	$\sigma \times 10^{-7}$ $(\Omega^{-1}cm^{-1})$	$Np \times 10^{15}$ (cm^{-3})	S (V/dec)	$N_{ss}^{max} \times 10^{12}$ $(eV^{-1}\ cm^{-2})$
PMMA	2.90	–8.5	5.6	1.22	11	4.7
CyEP	0.80	–9.0	2.9	2.38	18	39.0
Parylene-C	6.08	–10.0	1.1	0.12	7	3.7

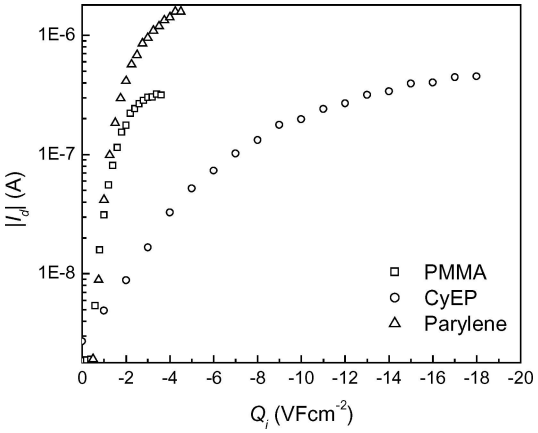

Figure 7 Transfer characteristics (normalized to the charge) of the quaterthiophene FETs fabricated using the different dielectrics PMMA, CyEP, Parylene-C.

A reduction in insulator thickness leads to an increase in the gate field E and the charge per unit area on the semiconductor side of the insulator [19]. It may be noted that the value of mobility for the parylene device is among the best so far reported for quaterthiophene [20–22]. This device exhibited the lowest subthreshold swing of 7 V/dec and consequently the lowest interfacial trap density, 3.7×10^{12} $eV^{-1}cm^{-2}$. The low polarity of parylene helps decrease the energetic disorder at the insulator-semiconductor interface, by decreasing the localized states due to the dipolar disorder [16].

To compare the performance of devices using gate dielectrics with different dielectric constants, normalization of the transfer characteristics to charge is required. The electrical charge Q_i induced by the gate insulator at the semiconductor-insulator interface in C/cm^2 is given by

$$Q_i = C_i V_s \tag{5}$$

Fig. 7 shows the I_d *vs.* Q_i plots at $V_d = -15$ V. The plots do not collapse on one another. It means that the performance of the 4T FETs with different dielectrics are mainly controlled by the quality of the dielectric-semiconductor interface.

4. Conclusions

We have investigated the performance of 4T FETs with three different gate dielectrics. The surface morphology, leakage currents, and the dielectric constant of the insulator film are crucial in the performance of the OFET. Of all the three insulators studied, parylene-C is found to be best suited for a gate dielectric in an OFET. The impressive performance of this device is attributed to its low leakage current and low energetic disorder at the semiconductor-insulator interface due to the low polarity. Modification of the surface and fabrication of thinner films of parylene would ensure better performance of these devices.

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